UNI-SEMICONDUCTOR CO.,LTD

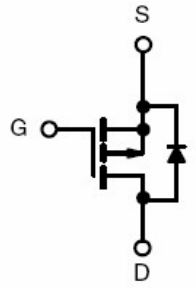
宇 力 半 导 体 有 限 公 司

AP25P06K Data Sheet

V 1.1

Description

The AP25P06K uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge .This device is well suited for high current load applications.



Schematic diagram

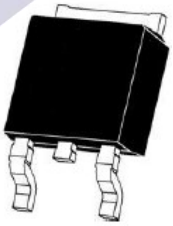
General Features

- V_{DS} =-60V,I_D =-25A
  $R_{DS(ON)}$ <60mΩ @ V_{GS}=-10V
  $R_{DS(ON)}$ <72mΩ @ V_{GS}=-4.5V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- High side switch for full bridge converter
- DC/DC converter for LCD display

Marking and pin assignment



TO-252 -2Ltop view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
25P06K	AP25P06K	TO-252			

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

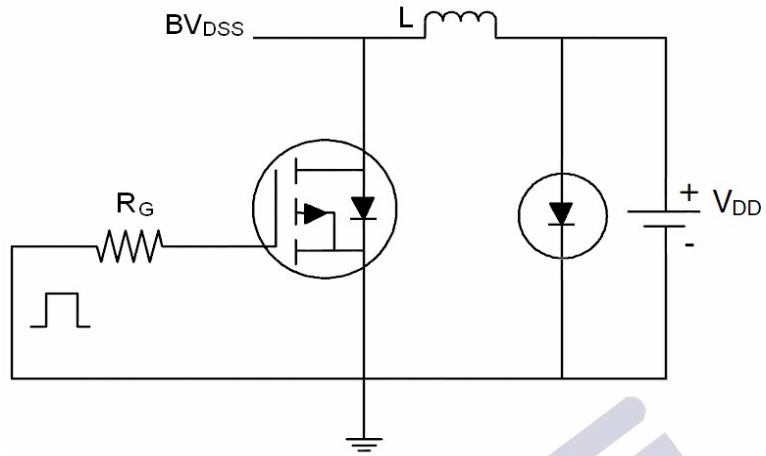
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	-25	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	-12.7	A
Pulsed Drain Current	I_{DM}	-72	A
Maximum Power Dissipation	P_D	60	W
Derating factor		0.4	W/℃
Single pulse avalanche energy (Note 5)	E_{AS}	50	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

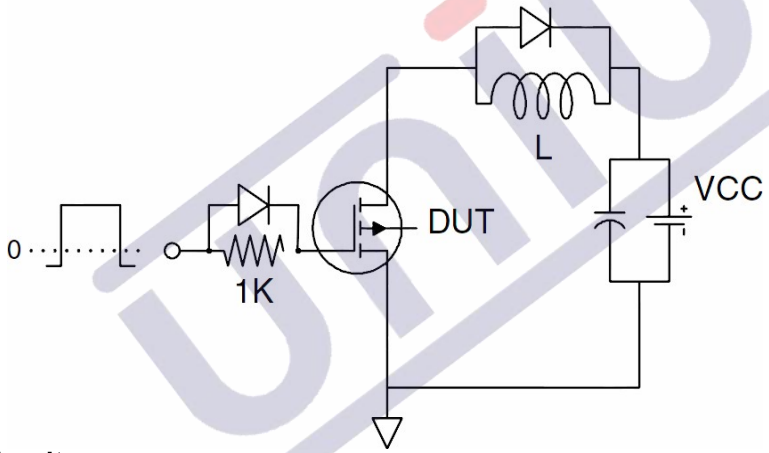
Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	2.5	℃/W

Test Circuit

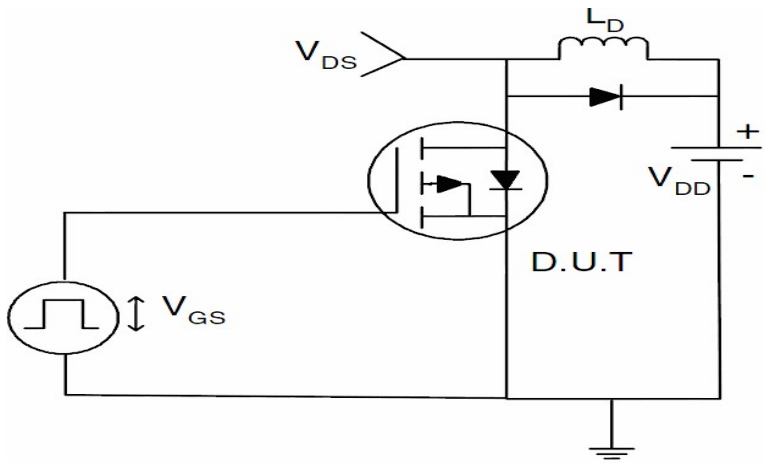
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



1.版本记录

DATE	REV.	DESCRIPTION
2018/04/19	1.0	First Release
2021/11/12	1.1	Layout adjustment

2.免责声明

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